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SF - 6547

B. E. II (Sem. IV) (I.T.) Examination

May / June – 2011

Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. 2 (SEM. 4) (I.T.)

Name of the Subject :

☛ DIGITAL CIRCUITS

☛ Subject Code No. : 6 5 4 7 ☛ Section No. (1, 2,.....) : Nil

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the extreme right indicate marks.
(4) Draw logic circuit for design problem.
(5) Assume necessary data.

1 (a) Answer the following : **10**

(1) What is digital system ? What are the advantages of digital system over analog system ?
(2) What is demultiplexer ?
(3) What is Parity Bit ? Draw 3 - bit parity generator circuit.
(4) Describe SOP and POS forms.
(5) Write the difference between truth table and excitation table ?

(b) Do as Directed : (any **four**) **10**

(1) Show that $A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$
(2) Convert $(A08F.EA)_{16}$ and $(8E47.AB)_{16}$ to decimal.
(3) Multiply $(10110)_2$ with $(10.1)_2$
(4) Convert $(2598.675)_{10}$ to Hexadecimal.
(5) Reduce using mapping the expression $\sum m(0,1,2,3,5,7,8,9,10,12,13)$ and implement it in universal logic.

2 (a) What is BCD number ? Explain BCD addition and a combinational circuit which can perform BCD addition. 8

(b) Explain half Adder/Substractor and full Adder/Substractor in detail. Also show their implementation using any one universal gate. 7

OR

(b) Write a short note on PLA. 7

3 Do as directed : (any **three**) 15

(1) Implement the following function with a MUX :

$F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$

(2) Explain Half/Full adder circuits. Also show their NAND gate implementation.

(3) What do you mean by universal gate ? Explain it in detail.

(4) Design a 4 - bit Binary - to - gray code converter circuit.

4 (a) Answer the following : 10

(1) What is state table ?

(2) State True/False : A+A=1.

(3) T Flip-flop is a single input version of _____ flip-flop.

(4) State True/False : The SET input can use of make Q as 0.

(5) 1 X 4 demultiplexer has _____ input,_____ output and _____ select lines.

(6) What is direct preset and direct clear ?

(7) State True/False : Gray code is error detecting code.

(8) An n - bit parity generator circuit needs _____ bit parity checker circuit.

(9) State True/False : SET input can use to make Q as 0.

(10) State True/False : OR gate is known as any or all.

(b) Attempt any **two** : 10

(1) Write difference between syncronous and asynchronous counter ?

(2) Explain Master - Slave flip - flop.

(3) Simplify the following Boolean function to a minimum number of literals.

$xyz + x'y + xyz'$

5 (a) Design BCD counter with JK flip - flops. 8

(b) Explain universal shift register. 7

OR

(b) What is flip - flop ? Discuss characteristics of various flip - flop. 7

6 Do as directed : (any **three**) 15

(1) Design and implement a mod - 6 asynchronous counter using T FFs.

(2) Design a circuit to convert S - R flip - flop to J - K flip - flop.

(3) Write about Johnson Counter.

(4) Design a D counter that goes through states 0, 1, 2, 3, 0,....
